

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**  
**(Case No. 15258US03)**

In the Application of:

Ahmadreza Rofougaran et al.

U.S. Serial No.: 09/695,715

Filed: October 23, 2000

For: ADAPTIVE RADIO TRANSCEIVER

Examiner: Marceau Milord


Group Art Unit: 2618

)  
) *Conf. No.:* 2742  
)

) *Customer No.:* 23446  
)

) **CERTIFICATE OF TRANSMISSION**  
)

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) April 12, 2007.  
)

)  
)   
) Michael T. Cruz  
) Reg. No. 44,636  
)

**RESPONSE TO NOTICE OF DRAWING  
INCONSISTENCY WITH SPECIFICATION**

Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

Sir:

This is a timely response to the Notice of Drawing Inconsistency with Specification mailed April 3, 2007 ("the Notice"), a copy of which is enclosed herein.

The Notice alleges that FIGS. 21-24 are contained in the Drawings, but are not listed in the Brief Description of the Drawings in the specification. Applicants respectfully disagree.

The specification at page 5, lines 22-29 discloses a brief description of FIGS. 21-24. Applicants have enclosed, as a courtesy, the specification at pages 5-6. It is therefore respectfully submitted that the Notice is in error and that a brief description of FIGS. 21-24 is provided in the specification at page 5, lines 22-29.

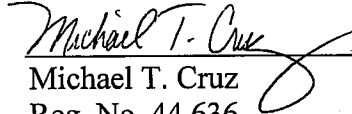
The Examiner may have misconstrued the Preliminary Amendment filed on October 23, 2000 ("the Preliminary Amendment"), a copy of which is enclosed herein, in which Applicants deleted the specification at page 5, lines 30-34, which also referred to FIGS. 21-22. However, the Preliminary Amendment did not amend the brief descriptions of FIGS. 21-24 in the specification at page 5, lines 22-29.

It is therefore respectfully requested that, since the Notice is in error, the Notice be withdrawn.

The Commissioner is hereby authorized to charge any additional fees, to charge any fee deficiencies or to credit any overpayments to the deposit account of McAndrews, Held & Malloy, Account No. 13-0017.

Dated: April 12, 2007

Respectfully submitted,

  
\_\_\_\_\_  
Michael T. Cruz  
Reg. No. 44,636

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15258US03 MSC



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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/695,715	10/23/2000	Ahmadreza Rofougaran	40593/CAG/B600	2742

EXAMINER	
MILORD, MARCEAU	

ART UNIT	PAPER NUMBER
2618	

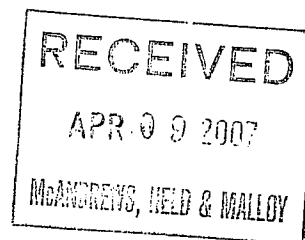
MAIL DATE	DELIVERY MODE
04/03/2007	PAPER

7590 04/03/2007  
CHRISTOPHER C. WINSLADE  
MCANDREWS, HELD & MALLOY  
500 W. MADISON STREET  
SUITE 3400  
CHICAGO, IL 60661

Please find below and/or attached an Office communication concerning this application or proceeding.

Corrected Drawings/Spec  
RESPONSE DUE:  
May 7, 2007

BT





## UNITED STATES PATENT AND TRADEMARK OFFICE

UNDER SECRETARY OF COMMERCE FOR INTELLECTUAL PROPERTY AND  
DIRECTOR OF THE UNITED STATES PATENT AND TRADEMARK OFFICE

### NOTICE OF DRAWING INCONSISTENCY WITH SPECIFICATION

The drawings filed 10/23/00 have been received. However, an inconsistency exists between the drawings and the Brief Description of the Drawings in the specification.

Figures        are listed in the Brief Description of the Drawings in the specification but not contained in the Drawings.

Figures 21-24 are contained in the Drawings but not listed in the Brief Description of the Drawings in the specification.

Applicant is required to correct the above-noted inconsistency within a time period of **ONE MONTH or THIRTY (30) DAYS, whichever is longer**, from the mailing date of this Notice, or within the time remaining in the time period set forth in the Notice of Allowability (Form PTOL-37) to file corrected drawings, whichever is longer. **NO EXTENSION OF THIS TIME PERIOD MAY BE GRANTED UNDER EITHER 37 CFR 1.136 (a) OR (b)**

Failure to correct the above noted inconsistency will result in **abandonment** of the application.

The file will be held in the Publishing Division to await the correction of the inconsistency.

**Return Corrected Drawings/Specification to:**

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P.O. Box 1450

Alexandria, VA 22313-1450

Office of Patent Publication/Publishing Division  
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1-888-786-0101

FORM PTO-1631 (REV. 10-03)

FIG. 18 is a clock generator in accordance with an exemplary embodiment of the present invention;

FIG. 19(a) is a graphical depiction of a clock signal spectrum input into the clock generator of FIG. 18 in accordance with an exemplary embodiment of the present invention;

FIG. 19(b) is a graphical depiction of a signal spectrum at the output of a two second stage polyphase filter of the clock generator of FIG. 18 in accordance with an exemplary embodiment of the present invention;

FIG. 19(c) is a graphical depiction of the signal spectrum output from a low pass filter of the clock generator of FIG. 18 in accordance with an exemplary embodiment of the present invention;

FIG. 19d is a block diagram of an exemplary polyphase filter;

FIG. 19e is a block diagram of a polyphase filter including a two-stage polyphase filter;

FIG. 19f is a schematic of an exemplary embodiment of a polyphase structure;

FIG. 19g is a schematic of a branch of the RC network of FIG. 19f

FIG. 20(a) is a graphical depiction of a signal spectrum at the input to a polyphase filter in accordance with an exemplary embodiment of the present invention;

FIG. 20(b) is a graphical depiction of a signal spectrum at the output of the polyphase filter in accordance with an exemplary embodiment of the present invention;

FIG. 20(c) is a graphical depiction of the signal spectrum output from a low pass filter of the polyphase filter in accordance with an exemplary embodiment of the present invention;

FIG. 21 is a block diagram of a demodulator in accordance with an exemplary embodiment of the present invention;

FIG. 22 is a block diagram of a differentiator of the demodulator of FIG. 21 in accordance with an exemplary embodiment of the present invention;

FIG. 23 is a block diagram of a multiplier of the demodulator of FIG. 21 in accordance with an exemplary embodiment of the present invention;

FIG. 24 is a block diagram of a peak detector/slicer of the demodulator of FIG. 21 in accordance with an exemplary embodiment of the present invention;

FIG. 21 is a system block diagram of a signal processing system operating in a real time fax relay mode in accordance with an exemplary embodiment of the present invention;

FIG. 22 is a diagram of the message flow for a fax relay in non error control mode in accordance with an exemplary embodiment of the present invention;

FIG. 23 is a flow diagram of a method for fax mode spoofing in accordance with an exemplary embodiment of the present invention;

5 FIG. 24 is a block diagram of several signal processing systems in the modem relay mode for interfacing between a switched circuit network and a packet based network in accordance with an exemplary embodiment of the present invention;

FIG. 25 is a block diagram of a differential power amplifier in accordance with an exemplary embodiment of the present invention;

10 FIG. 26(a) is a electrical diagram of one bias circuit to the input and/or output stage of the differential power amplifier of FIG. 25 in accordance with an exemplary embodiment of the present invention;

FIG. 26(b) is an electrical diagram of another bias circuit to the input and/or output stage of the differential power amplifier of FIG. 25 in accordance with an exemplary embodiment of the present invention;

15 FIG. 27 is an electrical diagram of a bias circuit for a the current source of the differential power amplifier of FIG. 25 in accordance with an exemplary embodiment of the present invention;

FIG. 28 is an electrical diagram of a power control circuit for the differential power amplifier of FIG. 25 in accordance with an exemplary embodiment of the present invention;

20 FIG. 29 is an electrical diagram of a single-ended differential power amplifier in accordance with an exemplary embodiment of the present invention;

FIG. 30(a) is an electrical diagram of digitally programmable CMOS power amplifier in accordance with an exemplary embodiment of the present invention;

25 FIG. 30(b) is a block diagram of an alternative embodiment of the transmitter and local oscillator generator of FIG. 2;

FIG. 30(c) is a block diagram of a CMOS offset PLL;

FIG. 30(d) is a block diagram of an offset PLL architecture utilizing a subsampling mixer;

FIG. 30(e) is a block diagram illustrating frequency conversion and an I/Q mixer circuit;

30 FIG. 30(f) illustrates a typical mixing process;

FIG. 30(g) illustrates a frequency conversion scheme that tends to minimize the adverse effects due to frequency pulling and additionally tends to provide the benefit of reduced power consumption;

35 FIG. 30(h) is a block diagram of a first embodiment of a subsampling mixer for high frequencies;

## IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

*I hereby certify that this correspondence is being deposited with the U.S. Postal Service as first class mail in an envelope addressed to Commissioner of Patents and Trademarks, Washington, D.C. 20231 on November 17, 2000.*

  
Elaine Johnson

Applicant : Ahmadreza Rofougaran et al.  
Filed : October 23, 2000  
Application  
No. : 09/695,715  
Title : AN ADAPTIVE RADIO TRANSCEIVER  
  
Grp./Div. : To be assigned  
Examiner : To be assigned  
Docket No. : 40593/CAG/B600

## PRELIMINARY AMENDMENT

Assistant Commissioner for Patents  
Washington, D.C. 20231

Post Office Box 7068  
Pasadena, CA 91109-7068  
November 17, 2000

Commissioner:

Please amend the above-identified patent application as follows:

**In the Specification**

Page 5, delete lines 30-34, beginning with "FIG. 21" and ending with "invention";.

Page 6, delete lines 3-7, beginning with "with" and ending with "invention";.

Page 7, line 17, after "33" insert -- (a) --;

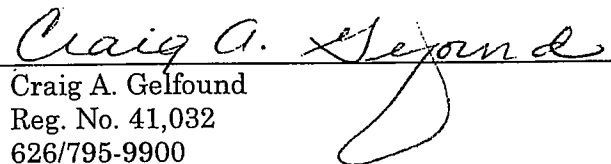
line 19, after "33" insert -- (b) --.

**REMARKS**

It is respectfully requested that the foregoing Preliminary Amendment be entered prior to examination of this application.

Respectfully submitted,

CHRISTIE, PARKER & HALE, LLP

By   
Craig A. Gelfound  
Reg. No. 41,032  
626/795-9900

CAG/ej  
EJ PAS284821.1\*-11/17/00 11:23 AM